Full-Chip Power Supply Noise Time-Domain Numerical Modeling and Analysis for Single and Stacked ICs

Li Zheng, Yang Zhang, *Student Member, IEEE*, and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*— In this paper, a distributed circuit model for on-die power distribution network in single and 3-D ICs is developed, and a set of difference equations are derived based on the circuit model and numerically solved using the finite-difference method. Both IR-drop and simultaneous switching noise, two components of power supply noise (PSN), are iteratively solved in time domain, thereby enabling a transient analysis of PSN. Under the assumptions that on-die power/ground pads, power density, and decoupling capacitors are uniformly distributed, PSN within a unit cell is accurately simulated with <1% error compared with HSPICE simulation. By reducing modeling grid fineness, the numerical modeling approach is applied to a full chip that has multiple blocks with nonuniform power/ground pads, power density, and decoupling capacitance density. Based on full-chip modeling, the PSN distribution of a two-die stack is simulated, and the impact of increasing decoupling capacitance and power/ground pads is investigated.**

***Index Terms*— 3-D ICs, finite-difference method, IR-drop, numerical modeling, power distribution network (PDN), power supply noise (PSN), simultaneous switching noise (SSN).**

I. Introduction

POWER supply noise (PSN) consists of IR-drop and simultaneous switching noise (SSN; or ΔI noise), which are due to the parasitic resistance, inductance, and decoupling capacitance of the power distribution network (PDN) [1]. The interactions of the board, package, and die-level PDNs cause noise of different frequency ranges, among which the mid-frequency noise caused by the package parasitic inductance and on-die decoupling capacitance has the largest magnitude and could degrade performance when it affects critical paths [2], [3]. Thus, mid-frequency noise is the focus of this paper.

Power delivery is becoming more challenging in today's high-performance computing systems due to the increasing device and power densities and decreasing supply voltage and clock cycle. The former causes larger PSN while the latter leads to smaller noise margin [4]. This trend is increasingly becoming challenging for modern ICs and, in particular, for the 3-D integration of high-power dice, since the required current would significantly increase, and through silicon vias (TSVs) add parasitic resistance and inductance to the on-die PDN, which would lead to an increase in PSN [5]. Thus, suppressing PSN is critical to the success of high-performance computing systems. An efficient and accurate PDN model would aid in answering what-if type questions during design space exploration and resource allocation for PSN suppression. This is critical to avoid overdesigning or underdesigning the PDN.

Various methods have been developed to model PDN and explore IR-drop and ΔI noise. A compact physical model for IR-drop is developed for chip/package codesign [6]. In [7], IR-drop is formulated using a finite volume method for electrical–thermal simulation. The work in [8] presents a distributed circuit model of a package and an on-die PDN for both the IR-drop and ΔI noise analysis but the circuit is for single IC and no specific method is provided to solve the circuit model. A compact physical model for IR-drop and ΔI noise is developed based on a distributed circuit model and frequency domain formulation in [9]. In [10], a finite-difference formulation based on a latency insertion method is used to simulate PSN in on-chip PDN for a single IC. A method combining electromagnetic and SPICE simulations is proposed in [11] for modeling and analyzing PDN performance. In [12], the PDN impedance of TSV-based 3-D ICs is extracted and analyzed based on the method developed in [11]. The work in [13] models and analyzes PDN impedance for the TSV-based 3-D integration using a lumped circuit model and a distributed circuit model. The above cited PDN modeling efforts either focus on the steady-state IR-drop or frequency domain impedance analysis and most efforts are for single IC. In this paper, and unlike existing efforts, the time-domain PDN noise, including resistive IR-drop and transient ΔI noise for a full 3-D chip stack, is simulated and analyzed based on a distributed circuit model and the finite-difference method. The contributions of this paper are threefolds. First, we develop a distributed circuit model focused on 3-D ICs to answer 'what-if' type questions for design space exploration in early design stage. Second, we validate the 3-D circuit model with HSPICE simulation, and the maximum error is <1%. Third, we explore the impact of on-chip decoupling capacitors (decaps) and TSVs on PDN noise suppression for a 3-D chip stack with multiple functional blocks of different power density and decoupling capacitance distributions.

This paper is organized as follows: Section II presents the numerical modeling method for on-die global PDN assuming

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The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: lizheng@gatech.edu; steven.zhang@gatech.edu; muhannad.bakir@mirc.gatech.edu).

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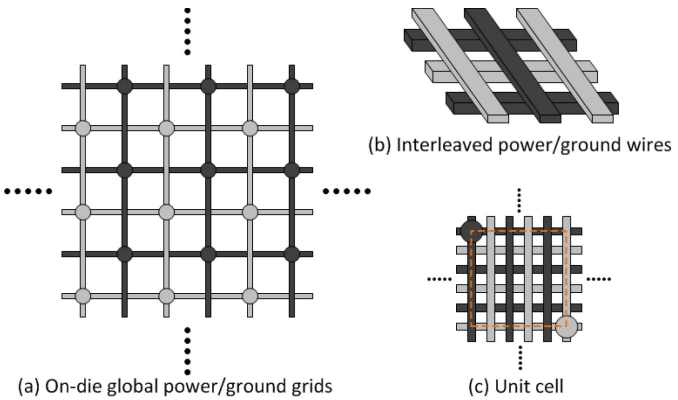

Fig. 1. (a) On-die global power/ground grids: power pads and grid segments (black colored), ground pads and grid segments (gray colored). (b) Interleaved structure of power/ground segments. (c) Unit cell (confined by a pair of power and ground pads).

uniform die parameters. In Section III, PSN of a single die and a 3-D die stack is simulated based on the model presented in Section II and validated with HSPICE. Section IV extends the distributed circuit model in Section II for full-chip modeling and accounting nonuniform die parameters. PSN of a two-die stack with blocks of different power densities is simulated. The impact of adding on-die decoupling capacitors and power/ground pads to the high-power blocks for PSN suppression is investigated. Section V concludes this paper.

II. Numerical Modeling of Uniform On-Die Power Distribution Network

In this section, PSN of a 3-D die stack is simulated and analyzed based on a distributed circuit model derived under assumptions of uniform power density, decoupling capacitor distribution, power/ground pads, and power/ground grids.

A. Modeling of On-Die Power Distribution Network

The on-die PDN consists of global and local networks. The global network distributes supply current across the die, and the local network delivers the supply current from the global network to the active devices. In this paper, the global network is modeled, since it contributes most of the parasitics [9].

Fig. 1(a) shows the global PDN of the top two metal layers of a die, which consists of power/ground grids with pads. The orthogonal power/ground grids are interleaved, as shown in Fig. 1(b). Under the uniform PDN assumption, which assumes that: 1) the power/ground pads are uniformly distributed; 2) the power density is uniformly distributed; 3) the on-die decoupling capacitance is uniformly distributed; and 4) the grid segments are uniform; the on-die PDN can be divided into many identical unit cells, as shown in Fig. 1(c). A unit cell is comprised of a quarter of the power pad, a quarter of the ground pad, and the grid segments in-between.

With the uniform PDN assumption, we can model the unit cell, since it fully represents the on-die PDN. Fig. 2 shows the modeling approach and circuit models for the nodes within the unit cell. First, the power/ground grids in a unit cell are separated into two isolated grids following the approach in [4] and [9], as shown in Fig. 2(a)–(c). Since the power and ground grids are identical, the same circuit model can be applied.

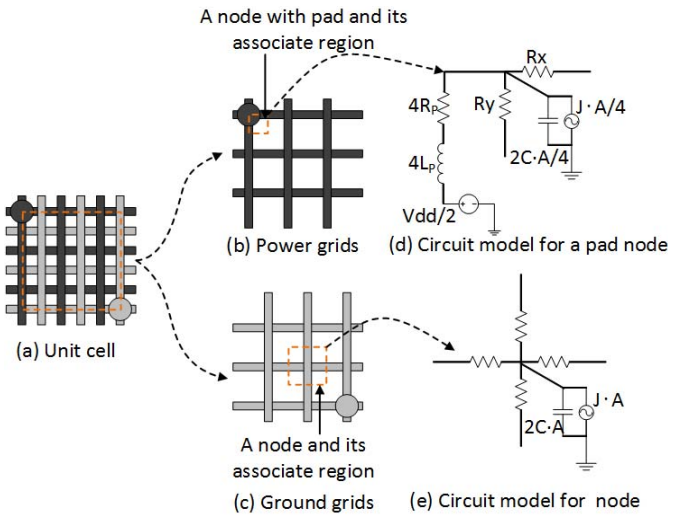

Fig. 2. Splitting of the power/ground grids of a unit cell to separate identical power grids and ground grids.

There are two types of nodes in the grid, which are the intersections of the grid segments. A pad node is a node at the corner of the grid and covered by a power/ground pad, while the remainder nodes represent the intersection of two orthogonal wires. Each node has neighboring nodes and an associated region with distributed decoupling capacitance and current drain (to represent gate activity), as shown in Fig. 2(b) and (c). Fig. 2(d) shows the circuit model for the pad node, which is connected to its two neighboring nodes with segment resistance R_x and R_y. C and J are the on-die decoupling capacitance density and current density, respectively. A is the area of the associated region of a node, which has four neighbors. Therefore, the associated decoupling capacitance and current of the pad node are $2 \cdot C \cdot A/4$ and $J \cdot A/4$, respectively. The decoupling capacitance density is multiplied by 2 because the decoupling capacitance in two grids is split. R_p and L_p are the resistance and inductance of the package-level PDN associated with each pad, respectively. Since only a quarter of the pad is included in a unit cell, it should be multiplied by 4. The supply voltage $V_{\rm dd}$ is divided by 2 because the power/ground grids are split into two identical grids.

Based on the above circuit models and Kirchhoff's circuit law, difference equations are derived to describe the voltage distribution over the grids. Equation (1) and (2) are for the circuit model in Fig. 2(d)

$$\frac{V(0,0,t)-V(\Delta x,0,t)}{R_x}+\frac{V(0,0,t)-V(0,\Delta y,t)}{R_y} = -J(t)\cdot\frac{\Delta x\cdot\Delta y}{4}-2C\cdot\frac{\Delta x\cdot\Delta y}{4} \cdot\frac{V(0,0,t)-V(0,0,t-\Delta t)}{\Delta t}-I_P(0,0,t) \quad (1)$$

$$V(0,0,t)+4R_P\cdot I_P(0,0,t)+4L_P \cdot\frac{I_P(0,0,t)-I_P(0,0,t-\Delta t)}{\Delta t}=\frac{V_{\rm dd}}{2} \quad (2)$$

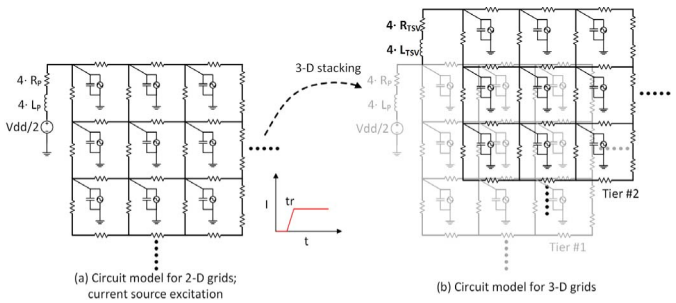

Fig. 3. (a) Distributed circuit model for a 2-D grids. (b) Extending the circuit model for 2-D grids to 3-D grids by integrating the resistance and inductance of TSVs.

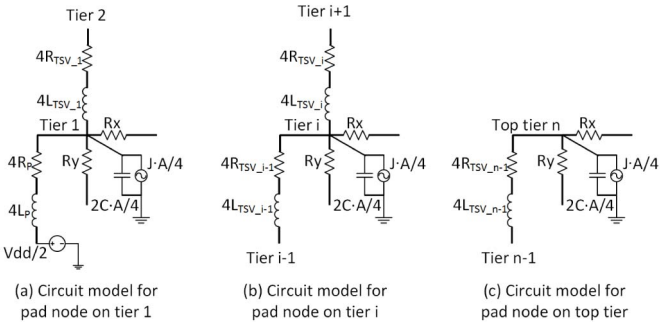

Fig. 4. Circuit model for the pad nodes in 3-D grids.

where $V(0,0,t)$ is the unknown voltage of the pad node at time t assuming that the pad node is at the origin, Δx and Δy are the segment lengths in x- and y-axes, respectively, $V(\Delta x,0,t)$ and $V(0,\Delta y,t)$ are the unknown voltages of the two neighbor nodes at time t, $J(t)$ is the current density at time t, C is the decoupling capacitance density, $(\Delta x\cdot\Delta y/4)$ is the associated region area of the pad node, $I_P(0,0,t)$ is the unknown current from the package to the pad node at time t, R_P is the package PDN resistance, L_P is the package PDN inductance, and $V_{\rm dd}$ is the chip supply voltage.

Similarly, difference equation (3) is derived using the circuit model for a regular node, as in Fig. 2(e)

$$\begin{aligned}&\frac{V(x,y,t)-V(x+\Delta x,y,t)}{R_x}\\&\quad+\frac{V(x,y,t)-V(x,y+\Delta y,t)}{R_y}\\&\quad+\frac{V(x,y,t)-V(x-\Delta x,y,t)}{R_x}\\&\quad+\frac{V(x,y,t)-V(x,y-\Delta y,t)}{R_y}\\&=-J(t)\cdot\Delta x\cdot\Delta y-2C\cdot\Delta x\cdot\Delta y\\&\quad\cdot\frac{V(x,y,t)-V(x,y,t-\Delta t)}{\Delta t}.\end{aligned}\tag{3}$$

Using the circuit models and the difference equations above, a distributed circuit model, as shown in Fig. 3(a), and a set of difference equations are derived for all nodes in the unit cell grid. The difference equations are numerically solved for the voltage distribution using the trapezoid scheme [14]. Since the voltage distribution is a function of time, it is iteratively solved as time advances with an initial current source excitation. In this paper, a simple step function of predefined rise time is used, as in Fig. 3(a). If omitting the time related terms in (1)–(3), the equations are appropriate to perform IR-drop simulations. In this paper, we focus on the time-domain transient ΔI noise.

B. Modeling of 3-D Power Distribution Network

In this section, we extend the 2-D distributed circuit model to grids in 3-D ICs. Fig. 3(b) shows the distributed circuit model for a two-tier die stack with TSV resistance and inductance. After integrating the TSV branch into the girds, the circuit models for the pad nodes on different tiers are shown in Fig. 4. Difference equations (4)–(6) are derived based on the new circuit models. The circuit model for the regular nodes (intersection of orthogonal wires) remains the same

$$\begin{aligned}&\frac{V_1(0,0,t)-V_1(\Delta x,0,t)}{R_x}+\frac{V_1(0,0,t)-V_1(0,\Delta y,t)}{R_y}\\&\quad=-J_1(t)\cdot\frac{\Delta x\cdot\Delta y}{4}-2C\cdot\frac{\Delta x\cdot\Delta y}{4}\\&\qquad\cdot\frac{V_1(0,0,t)-V_1(0,0,t-\Delta t)}{\Delta t}\\&\qquad-I_P(0,0,t)-I_{\rm TSV\_1}(0,0,t)\end{aligned}\tag{4}$$

$$\begin{aligned}&\frac{V_i(0,0,t)-V_i(\Delta x,0,t)}{R_x}+\frac{V_i(0,0,t)-V_i(0,\Delta y,t)}{R_y}\\&\quad=-J_i(t)\cdot\frac{\Delta x\cdot\Delta y}{4}-2C\cdot\frac{\Delta x\cdot\Delta y}{4}\\&\qquad\cdot\frac{V_i(0,0,t)-V_i(0,0,t-\Delta t)}{\Delta t}\\&\qquad-I_{{\rm TSV}\_i}(0,0,t)+I_{{\rm TSV}\_i-1}(0,0,t)\end{aligned}\tag{5}$$

$$\begin{aligned}&V_i(0,0,t)-V_{i-1}(0,0,t)\\&\quad=4R_{\rm TSV}\cdot I_{{\rm TSV}\_i-1}(0,0,t)+4L_{\rm TSV}\\&\qquad\cdot\frac{I_{{\rm TSV}\_i-1}(0,0,t)-I_{{\rm TSV}\_i-1}(0,0,t-\Delta t)}{\Delta t}\end{aligned}\tag{6}$$

where $V_i(0,0,t)$ is the unknown voltage of the pad node on tier $i(>1)$ at time t, $I_{{\rm TSV}\_i}(0,0,t)$ is the unknown current of the TSV branch on tier i at time t, and $R_{\rm TSV}$ and $L_{\rm TSV}$ are the TSV resistance and inductance, respectively. Since a unit cell only possesses a quarter of TSV, $R_{\rm TSV}$ and $L_{\rm TSV}$ should be multiplied by 4 in the unit cell model. Here, we use a resistor and inductor model for TSVs without too much loss in accuracy [12], but complex models, such as Resistance, Inductance, Conductance, and Capacitance for TSVs, could be easily inserted into the circuit model.

III. Power Supply Noise Analysis Based on the Unit Cell Modeling and Simulation

Using the unit cell model developed Section II, PSN of a four-die stack is simulated and analyzed in this section. The simulation parameters used for the die stack are listed in Table I. We assume a homogeneous 3-D integration in which all dice in the stack are the same.

TABLE I
SIMULATION PARAMETERS OF THE 3-D DIE STACK

Parameter	Value	Parameter	Value
No. of stacked dice	4	segment length	28.3 μm
Die thickness (TSV height)	50 μm	segment width	2 μm
TSV diameter	7 μm	segment thickness	1 μm
Unit cell size	84 × 84 μm^2	Package inductance	0.5 nH
Pad/TSV pitch	118.8 μm	Package resistance	0.01 Ω
On-die current density	1 A/mm^2	Current rise time	0.1 ns
On-die decoupling capacitance density	5.3 nF/mm^2	Δt	0.01 ns
Grid fineness	11 × 11	Vdd	1 V

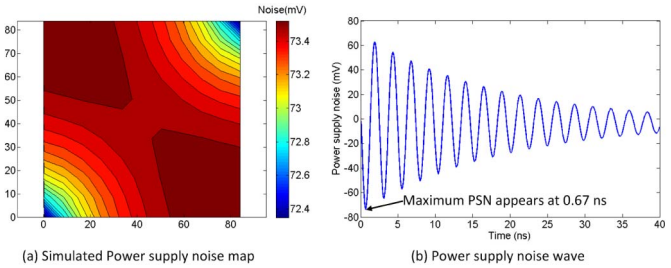

Fig. 5. (a) Simulated PSN map of a 2-D unit cell at 0.67 ns. (b) PSN wave at no-pad corners (upper left and lower right). The maximum PSN is 73.6 mV at 0.67 ns.

The size of the unit cell is 84 × 84 μm^2 with a pad/TSV pitch of 118.8 μm (distance between a pair of power and ground pads at two opposite corners of a unit cell). The grid fineness is defined as the number of intercrossing wires in the grids, which determines the number of nodes in the grids. The maximum on-die current density is 1 A/mm^2. In the simulation, we assume the current drain rises from 0 to 1 A/mm^2 linearly in 0.01 ns and all dice in the stack start switching at the same time. This would emulate the worst case PSN.

First, PSN of a single chip is simulated. Fig. 5(a) shows the simulated PSN map of the unit cell, which is symmetric along the two diagonals. The lower-left and upper-right corners have the smallest PSN because they are covered by the power and ground pads, which are connected to the package directly. PSN increases away from the power and ground pads due to additional parasitics of the on-die grids. Therefore, the upper-left and lower-right corners have the largest PSN. Fig. 5(b) shows the PSN waveform at the upper-left and lower-right corners. The fluctuation is caused by the interaction of the on-die decoupling capacitance and package inductance, and the damping magnitude is due to the resistive parasitics. The largest PSN magnitude of 73.6 mV appears at 0.67 ns assuming that the current begins to rise at 0 s.

In the four-die stack, the top die has the largest PSN because of the longest TSVs [15]. Fig. 6 shows the PSN map of the top die and PSN waveform at the upper-left and lower-right corners with no pad/TSV. The PSN distribution pattern is the same as that of 2-D case. The largest PSN magnitude is 161.2 mV, ∼120% increase due to 3-D stacking. The largest PSN appears at 1.36 ns.

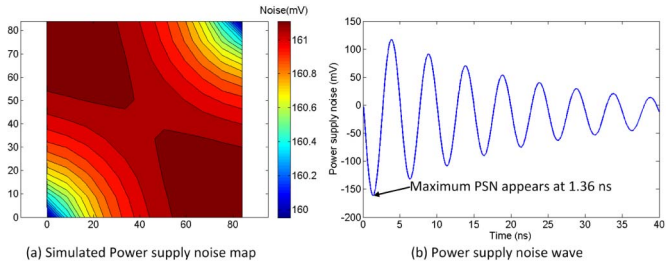

Fig. 6. (a) Simulated PSN map of the upper unit cell in a four-tier stack at 1.36 ns. (b) PSN wave at no-TSV corners (upper left and lower right). The maximum PSN is 161.2 mV at 1.36 ns.

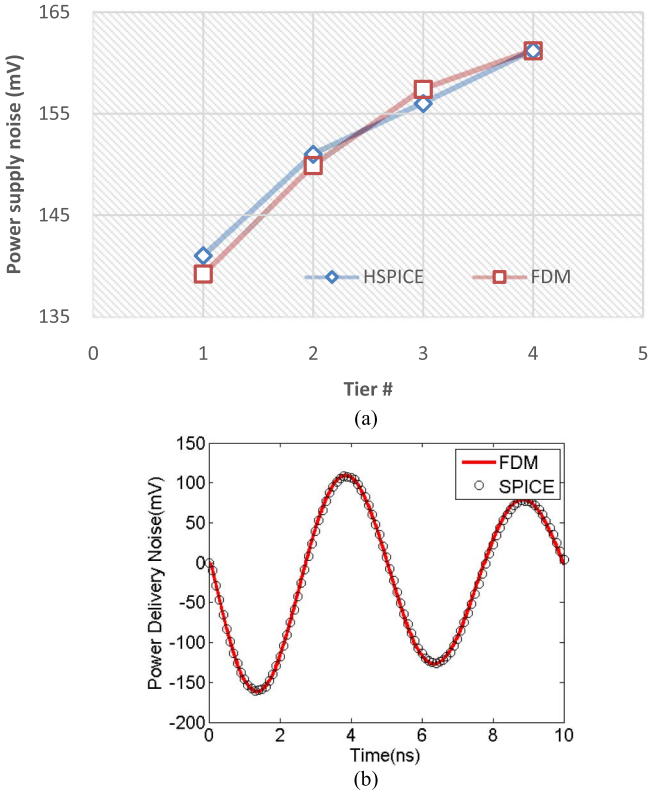

Fig. 7. (a) PSN simulation for the four-tier stack using FDM and HSPICE. (b) Transient noise waveform comparison of the no-TSV corners.

The simulation results of the four-die stack are verified with HSPICE, as shown in Fig. 7. The difference is <1% between our time-domain finite-difference method-based simulation and HSPICE simulation. The transient noise waveform is also compared at no-TSV corners and the maximum error is <3.5%, as shown in Fig. 7(b). Since the analysis and optimization of the simulation speed and memory usage of the model are not the focus of this paper, we leave these discussions for future work.

Next, the impact of the grid fineness on PSN simulation is investigated. Fig. 8 shows the PSN of each tier in the four-die stack with a different grid fineness. All other parameters are the same as listed in Table I. There is a relatively small difference in PSN when the grid fineness decreases from 11 × 11 to 6 × 6, as shown in Fig. 8. The difference is <1% when the grid fineness is further reduced to 2 × 2, which only considers the segments at the edges of the unit cell.

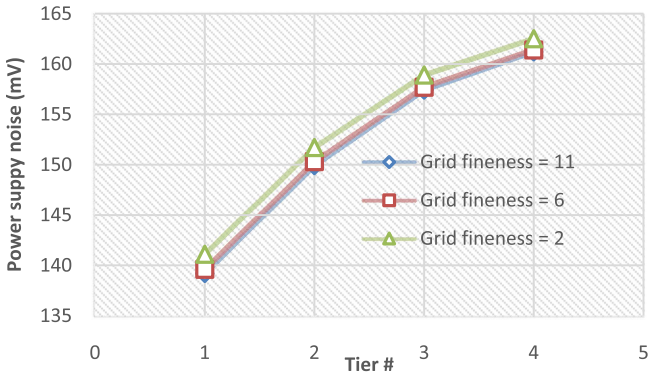

Fig. 8. PSN of each tier in the four-tier stack with a different grid fineness.

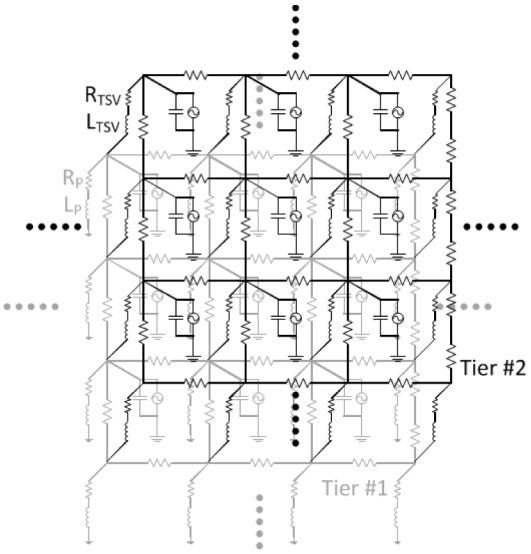

Fig. 9. Distributed 3-D circuit model for full die stack.

This indicates that we can significantly reduce the number of nodes for a unit cell with a small accuracy loss, which would enable full-die simulation and is discussed Section IV.

IV. Full-Die Nonuniform Power Distribution Network Simulation and Analysis

In this section, the distributed circuit model and difference equations are derived for a full die with multiple blocks of different decoupling capacitances and power densities based on the method described Section II. The PSN of a two-die stack is simulated, and the impact of adding decoupling capacitors and power/ground pads is analyzed.

A. Modeling of Full-Die Power Distribution Network

Fig. 9 shows the distributed circuit model for a two-die stack. Different from the unit cell circuit model, each node in this circuit model is connected to a pad/TSV. Different values of decoupling capacitance and current can be assigned to each node to account for the nonuniform distribution of decoupling capacitance and current.

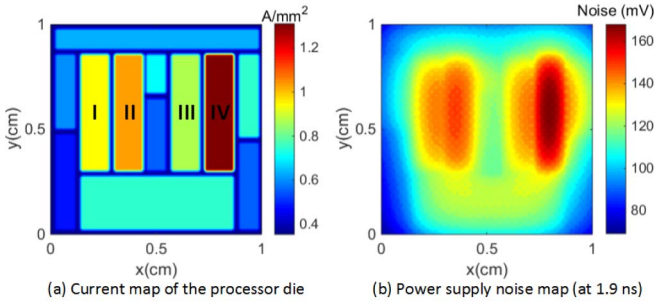

Fig. 10. (a) Current map of the processor die. (b) PSN map of the processor die at (maximum PSN 169.9 mV at 1.9 ns).

Based on the circuit model, difference equations for the node on tier i are derived as follows:

$$\begin{aligned}&\frac{V_{i,k}(x,y,t)-V_{i,k}(x+\Delta x,y,t)}{R_x}\\&\quad+\frac{V_{i,k}(x,y,t)-V_{i,k}(x,y+\Delta y,t)}{R_y}\\&\quad+\frac{V_{i,k}(x,y,t)-V_{i,k}(x-\Delta x,y,t)}{R_x}\\&\quad+\frac{V_{i,k}(x,y,t)-V_{i,k}(x,y-\Delta y,t)}{R_y}\\&=-J_{i,k}(x,y,t)\cdot\Delta x\cdot\Delta y-2C_{i,k}(x,y,t)\cdot\Delta x\cdot\Delta y\\&\quad\cdot\frac{V_{i,k}(x,y,t)-V_{i,k}(x,y,t-\Delta t)}{\Delta t}\\&\quad+I_{\mathrm{TSV}\_i-1,k}(x,y,t)-I_{\mathrm{TSV}\_i,k}(x,y,t)\end{aligned}\tag{7}$$

$$\begin{aligned}V_{i,k}(x,y,t)-V_{i-1,k}(x,y,t)&=4R_{\mathrm{TSV}}\cdot I_{\mathrm{TSV}\_i-1,k}(x,y,t)\\&\quad+4L_{\mathrm{TSV}}\cdot\frac{I_{\mathrm{TSV}\_i-1,k}(x,y,t)-I_{\mathrm{TSV}\_i-1}(x,y,t-\Delta t)}{\Delta t}\end{aligned}\tag{8}$$

where $V_{i,k}(x,y,t)$ is the voltage of node in block k on tier i, since a die has multiple blocks, $I_{\mathrm{TSV}\_i-1,k}(x,y,t)$ is the current flowing from tier $i-1$ to tier i through the TSV, and $I_{\mathrm{TSV}\_i,k}(x,y,t)$ is the current flowing from tier i to tier $i+1$.

B. Full-Die Power Supply Noise Simulation and Analysis

The PSN of a die with multiple blocks is simulated using the full-die model described Section IV.A. The block layout and power map are based on an Intel i7 processor [16], [17]. The die size is 1 cm × 1 cm, and the total power is 74.49 W. Fig. 10(a) shows the current density distribution assuming a supply voltage of 1 V. Blocks I–IV, which have relative large current/power density, are labeled. Block IV has the largest current density, which is greater than 1.2 A/mm^2. Except for the current/power distribution, other parameters of the power grid are the same as those listed in Table I.

Fig. 10(b) shows the simulated PSN map for a single processor die. As expected, large current density leads to large PSN. The maximum PSN is 169.9 mV at 1.9 ns in Block IV.

Next, two such high-power dice are stacked using TSVs. The parameters in Table I are used as the baseline case. Since the two stacked dice are identical, their PSN pattern

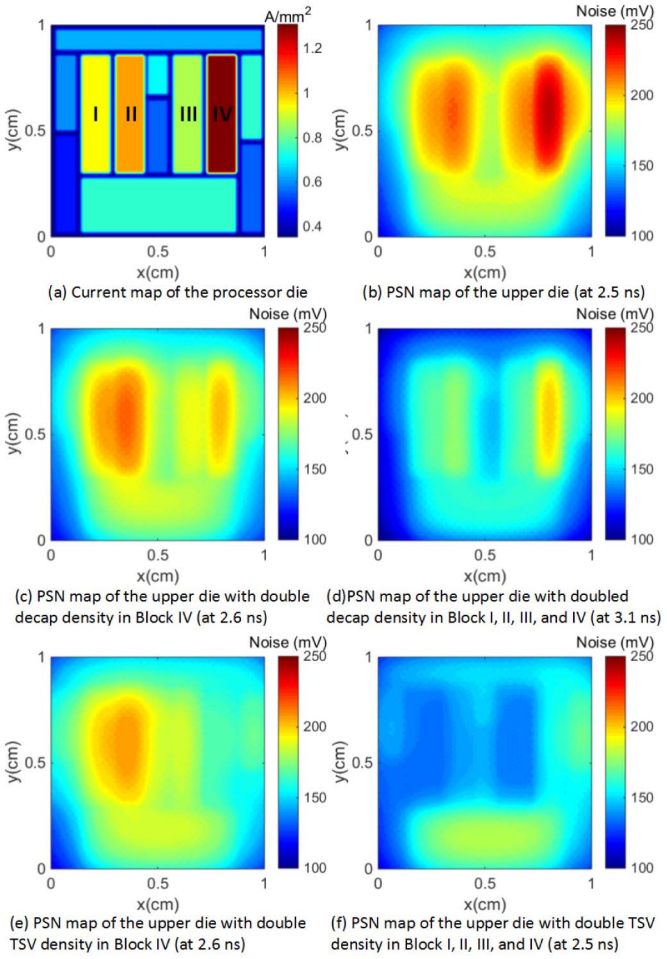

Fig. 11. (a) Current map of the logic die (with four high current blocks labeled). (b) PSN map of the upper die (maximum PSN 249.1 mV at 2.5 ns). (c) PSN map of the upper die with doubled decoupling capacitance density in Block IV (maximum PSN 219 mV at 3.2 ns). (d) PSN map of the upper die with doubled decoupling capacitance density in Blocks I–IV (maximum PSN 207 mV at 3.2 ns). (e) PSN map of the upper die with doubled TSV density in Block IV (maximum PSN 210.2 mV at 2.6 ns). (f) PSN map of the upper die with doubled TSV density in Blocks I–IV (maximum PSN 183 mV at 2.6 ns).

is the same. Fig. 11(b) shows the simulated PSN map of the upper die, which has a larger PSN than the lower die. The largest PSN increases to 242.8 mV, a 43% increase compared with the single-die case.

Besides the nonuniform distribution of power/current density, we can apply nonuniform decoupling capacitance and power/ground pad distributions using the full-die model. Increasing on-die decoupling capacitance and the number of power/ground pads are two effective ways of suppressing PSN [18]. The impact of doubling decoupling capacitance density and the number of power/ground pads for the high-power blocks in the two-die stack are investigated.

First, the decoupling capacitance density of Block IV is doubled for both dice in the stack while keeping all other parameters unchanged. Fig. 11(c) shows the PSN map of the upper die. PSN of Block IV is suppressed, and the maximum PSN occurs in Block II now, which has the second largest current density. Compared with the baseline case, the maximum PSN is suppressed to 218.1 mV, ∼10.2% reduction.

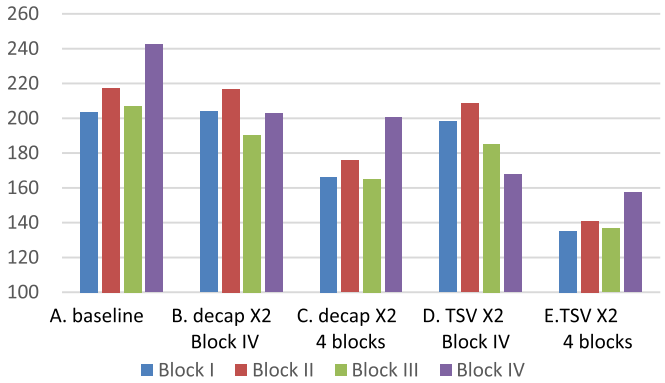

Fig. 12. PSN at the center point of the four blocks for the five scenarios.

Next, we double the decoupling capacitance density in all four labeled blocks. In this case, the PSN is suppressed to 201 mV, ∼17.2% reduction, as in Fig. 11(d). Fig. 11(e) shows the PSN map of the upper die with the doubled number of TSVs (power/ground pads) in Block IV. The PSN of Block IV is well suppressed, and the maximum PSN now occurs in Block II. The maximum PSN of the die decreases to 209.4 mV, ∼13.8% reduction. Next, the number of TSVs is doubled in all four blocks. The PSN is suppressed, and the maximum PSN is no longer in the four high-power density Blocks I–IV, as shown in Fig. 11(f). The maximum PSN is reduced to 183.1 mV, ∼24.6% reduction.

In the above analysis, the maximum PSN of the stack is compared for five different scenarios (A: baseline case; B: doubling decoupling capacitance in Block IV; C: doubling decoupling capacitance in all four blocks; D: doubling the TSVs in Block IV; and E: doubling the TSVs in all four blocks). Fig. 12 compares the PSN of the center point of the four blocks for the five different scenarios. Comparing scenarios B and D with A, doubling decoupling capacitance and TSVs in Block IV suppresses the PSN of Block IV (16.3% reduction in PSN) and the adjacent Block III (8.1% reduction) but has limited impact on Blocks I and II. Comparing scenarios B and C, further doubling decoupling capacitance in Blocks I–III significantly suppresses the PSN of the corresponding blocks but has minimal impact on Block IV, achieving 17%–20% reduction in PSN for the four blocks. Doubling the TSVs in all four blocks achieves ∼35% reduction in PSN for the four blocks, as in scenario E.

V. Conclusion

Time-domain PSN, including IR-drop and SSN, is accurately simulated for a unit cell under uniformity assumptions based on a distributed circuit model using a numerical modeling method. The circuit model is further extended for a full-chip 3-D stack simulation with no uniformity constraints. The PSN of a two-die stack with multiple blocks is simulated and analyzed. Adding decoupling capacitors or pads to the high-power blocks suppresses the PSN of the block and its adjacent regions. Doubling decoupling capacitance in the four blocks results in 17%–20% reduction in PSN for the blocks, while doubling TSVs density results in ∼35% reduction in PSN.

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Li Zheng received the B.S. degree from Zhejiang University, Hangzhou, China, in 2006, the M.S. degree from Shanghai Jiao Tong University, Shanghai, China, in 2009, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2015.

His current research interests include power delivery, microfluidic cooling, and advanced packaging for high-performance 3-D integrated systems.

Yang Zhang (S'13) received the B.S. degrees in microelectronics and math from Peking University, Beijing, China, in 2012. He is currently pursuing the Ph.D. degree in electrical engineering with the Georgia Institute of Technology, Atlanta, GA, USA.

Muhannad S. Bakir received the B.E.E. degree from Auburn University, Auburn, AL, USA, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 2000 and 2003, respectively.

He is currently an Associate Professor with the School of Electrical and Computer Engineering at Georgia Tech.